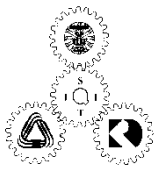


Sirindhorn International Institute of Technology

Thammasat University at Rangsit

School of Information, Computer and Communication Technology

ECS371: Practice Problems for the Final Examination

COURSE : ECS371 (Digital Circuits)
DATE : October 1, 2009
SEMESTER : 1/2009
INSTRUCTOR: Dr. Prapun Suksompong
TIME : 13:30-16:30
PLACE : BKD 32XX

Name		ID	
Section	CS or IT (circle one)	Seat	

Instructions:

1. Including this cover page, this exam has 12 pages.
2. **Read the questions carefully**.
3. Write your **first name and ID** on each page of your examination paper.
4. Write all your work in the space provided. You may not get full credit even when your answer is right without all of your work written down.
5. Closed book. Closed notes. No calculator.
6. Allocate your time wisely.
7. Do not cheat. The use of communication devices including mobile phones is prohibited in the examination room.
8. Your scores will depend strongly on the clarity and completeness of your solutions.
9. **Do not panic.**
10. Dr. Prapun will visit each exam room regularly. In general, there is no need to ask the proctor to call for Dr. Prapun.

The full score for this exam is XXX.

Part A: TRUE/FALSE.

Write 'T' if the statement is true and 'F' if the statement is false. If the statement is false, explain why. Put your answers/explanations in the table given below. (x pt)

1. A latch has two stable states.
2. A latch is considered to be in the SET state when the Q output is LOW.
3. A gated D latch must be enabled in order to change state.
4. An edge-triggered D flip-flop changes state whenever the D input changes.
5. A clock input is necessary for an edge-triggered flip-flop.
6. When both the J and K inputs are HIGH, an edge-triggered J-K flip-flop changes state on each clock pulse.
7. In an asynchronous counter, all flip-flops change state at the same time.
8. In a synchronous counter, all flip-flops are clocked simultaneously.
9. An asynchronous counter is also known as a ripple counter.
10. A decade counter has sixteen states.
11. Two cascaded decade counters divide the clock frequency by 20.
12. A counter with a truncated sequence has less than its maximum number of states.
13. To achieve a modulus of 100, ten decade counters are required.
14. Shift registers consist of an arrangement of flip-flops.
15. Two functions of a shift register are data storage and data movement.
16. In a serial shift register, several data bits are entered at the same time.
17. All shift registers are defined by specified sequences.
18. A shift register can have both parallel and serial outputs.
19. A data byte consists of eight bits.
20. A memory cell can store a byte of data.
21. The write operation stores data in memory.
22. The read operation always erases the data byte.
23. RAM is a *random address memory*.
24. Stored data is lost if power is removed from a static RAM.
25. Dynamic RAMs must be-periodically refreshed to retain data.
26. ROM is a random output memory.
27. The Nyquist frequency is twice the sampling frequency
28. A higher sampling rate is more accurate than a lower sampling rate for a given analog signal

Question	T/F	Explanation
1		

Part B: MULTIPLE CHOICE.

Choose the one alternative that **best** completes the statement or answers the question. Put your answers in the table given below. (X pt)

29. If an S-R latch has a 1 on the S input and a 0 on the R input and then the S input goes to 0, the latch will be
    (a) set (b) reset (c) invalid (d) clear
30. The invalid state of an S-R latch occurs when
    (a) S = 1, R = 0 (b) S = 0, R = 1 (c) S = 1, R = 1 (d) S = 0, R = 0
31. The purpose of the clock input to a flip-flop is to
    (a) clear the device
    (b) set the device
    (c) always cause the output to change states
    (d) cause the output to assume a state dependent on the controlling (S-R, J-K, or D) inputs.
32. For an edge-triggered D flip-flop,
    (a) a change in the state of the flip-flop can occur only at a clock pulse edge
    (b) the state that the flip-flop goes to depends on the D input
    (c) the output follows the input at each clock pulse
    (d) all of these answers
33. A feature that distinguishes the J-K flip-flop from the S-R flip-flop is the
    (a) toggle condition (b) preset input
    (c) type of clock (d) clear input
34. A J-K flip-flop with J = 1 and K = 1 has a 10 kHz clock input. The Q output is
    (a) constantly HIGH (b) constantly LOW
    (c) a 10 kHz square wave (d) a 5 kHz square wave
35. Asynchronous counters are known as
    (a) ripple counters (b) multiple clock counters
    (c) decade counters (d) modulus counters
36. An asynchronous counter differs from a synchronous counter in
    (a) the number of states in its sequence (b) the method of clocking
    (c) the type of flip-flops used (d) the value of the modulus
37. The modulus of a counter is
    (a) the number of flip-flops
    (b) the actual number of states in its sequence
    (c) the number of times it recycles in a second
    (d) the maximum possible number of states
38. A 3-bit binary counter has a maximum modulus of
    (a) 3 (b) 6 (c) 8 (d) 16
39. A 4-bit binary counter has a maximum modulus of
    (a) 16 (b) 32 (c) 8 (d) 4
40. A modulus-12 counter must have
    (a) 12 flip-flops (b) 3 flip-flops
    (c) 4 flip-flops (d) synchronous clocking

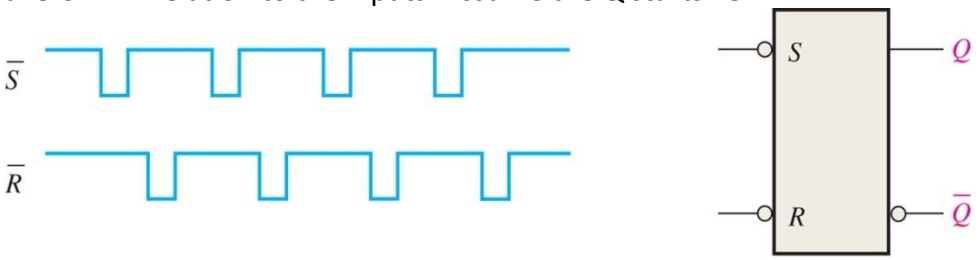
41. Which one of the following is an example of a counter with a truncated modulus?
    (a) Modulus 8 (b) Modulus 14 (c) Modulus 16 (d) Modulus 32
42. A BCD counter is an example of
    (a) a full-modulus counter
    (b) a decade counter
    (c) a truncated-modulus counter
    (d) answers (b) and (c)
43. Three cascaded modulus-10 counters have an overall modulus of
    (a) 30
    (c) 1000
    (b) 100
    (d) 10,000
44. The group of bits 10110101 is serially shifted (right-most bit first) into an 8-bit parallel output shift register with an initial state of J 1100100. After two clock pulses, the register contains
    (a) 01011110
    (e) 01111001
    (b) 10110101
    (d) 00101101
45. The bit capacity of a memory that has 1024 addresses and can store 8 bits at each address is
    (a) 1024 (b) 8192 (c) 8 (d) 4096
46. Data are stored in a random-access memory (RAM) during the
    (a) read operation (b) enable operation
    (c) write operation (d) addressing operation
47. Data that are stored at a given address in a random-access memory (RAM) is lost when
    (a) power goes off (b) the data are read from the address
    (c) new data are written at the address (d) answers (a) and (c)
48. A ROM is a
    (a) nonvolatile memory (b) volatile memory
    (c) read/write memory (d) byte-organized memory
49. A memory with 256 addresses has
    (a) 256 address lines (b) 6 address lines
    (c) 1 address line (d) 8 address lines
50. A byte-organized memory has
    (a) I data output line (b) 4 data output lines
    (c) 8 data output lines (d) 16 data output lines
51. A DRAM must be
    (a) replaced periodically (b) refreshed periodically
    (c) always enabled (d) programmed before each use
52. VHDL is a type of
    (a) programmable logic
    (c) programmable array
    (b) hardware description language
    (d) logical mathematics

53. In VHDL, a port is
    (a) a type of entity
    (b) an input or output
    (c) a type of architecture
    (d) a type of variable
54. A VHDL component
    (a) can be used once in each program
    (b) is a predefined description of a logic function
    (c) can be used multiple times in a program
    (d) is part of a data flow description
    (e) answers (b) and (c)
55. A VHDL component is called for use in a program by using a
    (a) signal
    (b) variable
    (c) component instantiation
    (d) architecture declaration

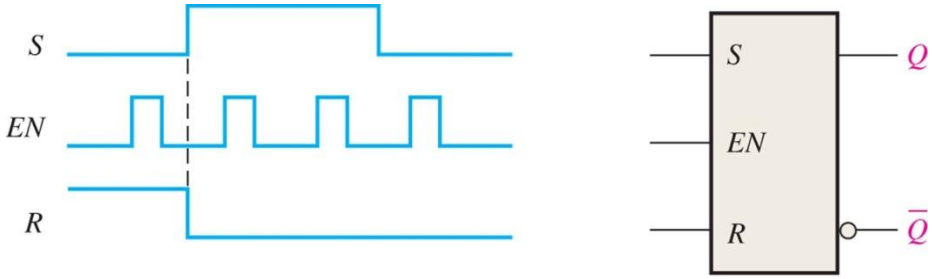
Question	Answer
29	

Part C

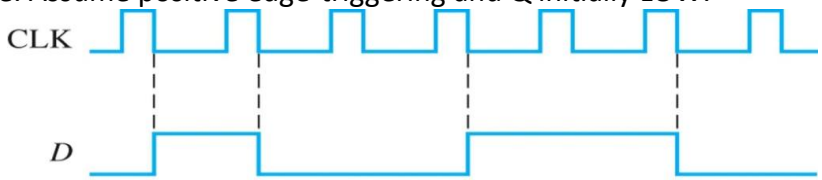
56. If the following waveforms are applied to an active-LOW S-R latch, draw the resulting Q output waveform in relation to the inputs. Assume the Q starts LOW.



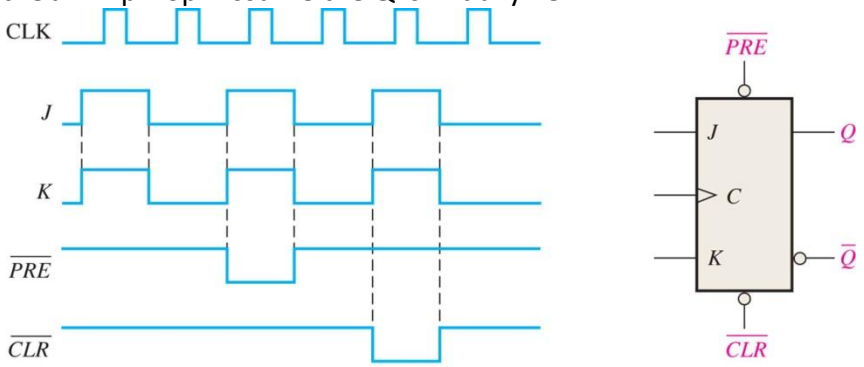
57. For a gated S-R latch, draw the resulting Q output waveform in relation to the inputs. Assume the Q starts LOW.



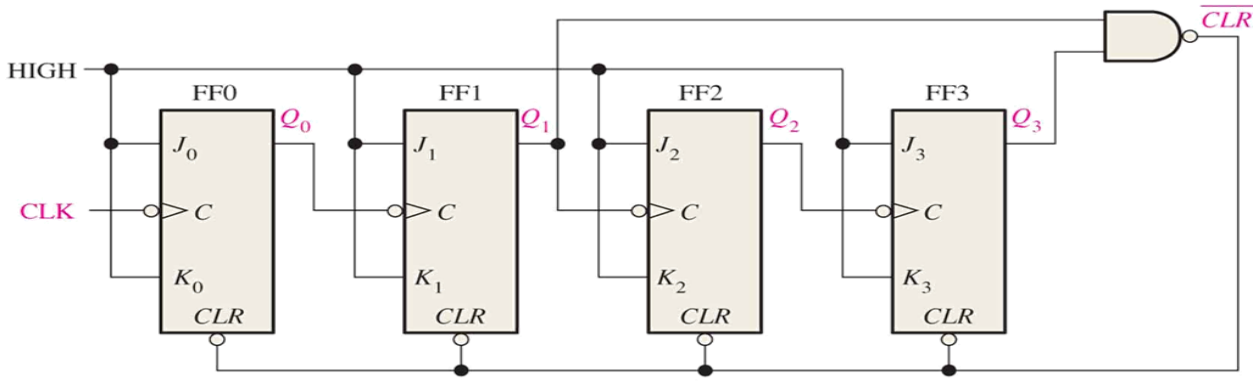
58. How can a latch be used as a contact-bounce eliminator?
59. Draw the Q output relative to the clock for a D flip-flop with the inputs as shown in the following figure. Assume positive edge-triggering and Q initially LOW.



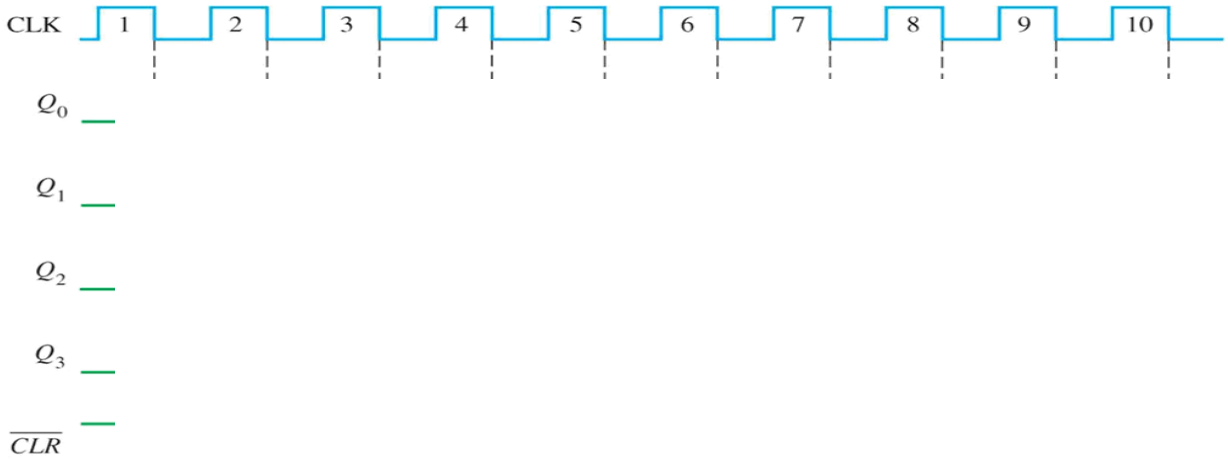
60. Determine the Q waveform relative to the clock of the signals shown below are applied to the inputs of the J-K flip-flop. Assume the Q is initially LOW.



61. What are the differences between synchronous and asynchronous counters?
62. Determine the output wave form of the following counter.



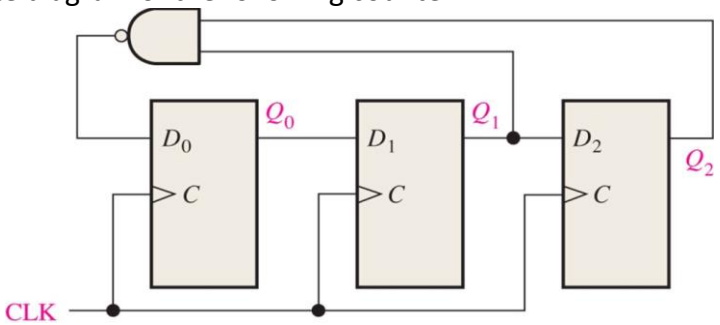
Assume that the Q start with LOW vale.



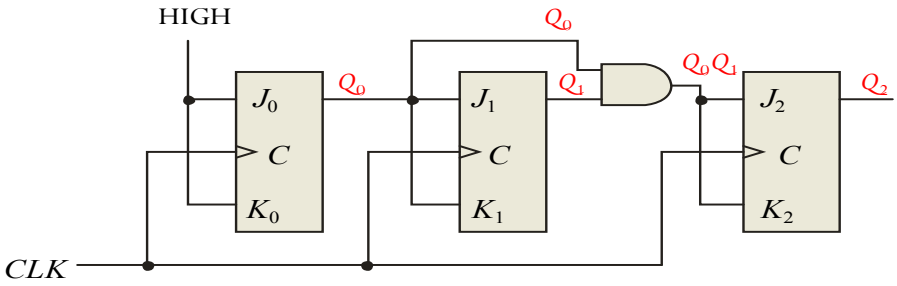
Will there be any glitches on the output? Why and where would them be? Explain.

63. Show how to connect a 74LS93 4-bit asynchronous counter for each of the following moduli.
    a. 9
    b. 11
    c. 13
    d. 14
    e. 15

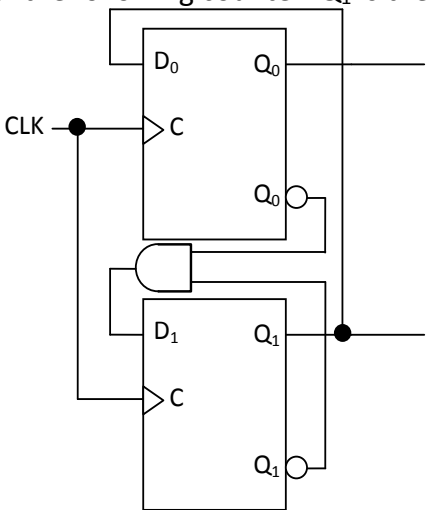
64. Determine the state diagram of the following counter



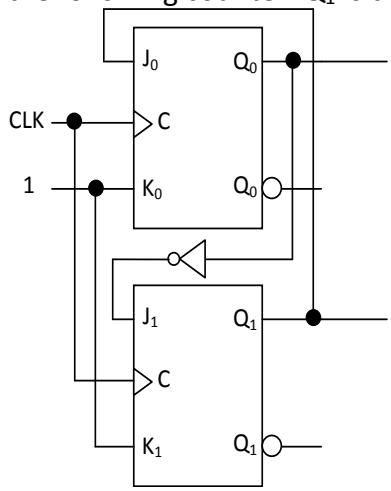
65. Determine the state diagram of the following counter



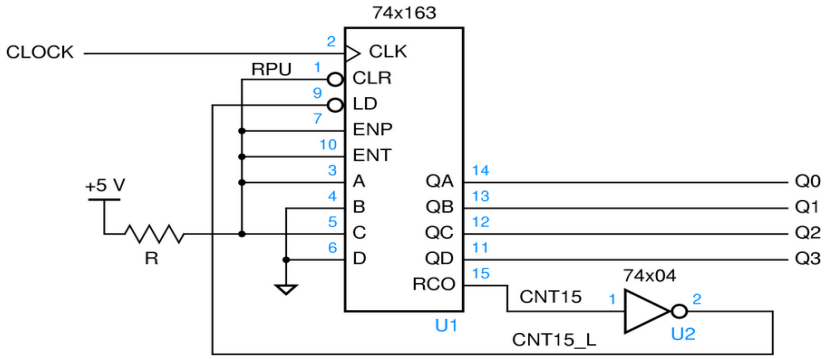
66. Determine the state diagram of the following counter. Q_1 is the MSB.



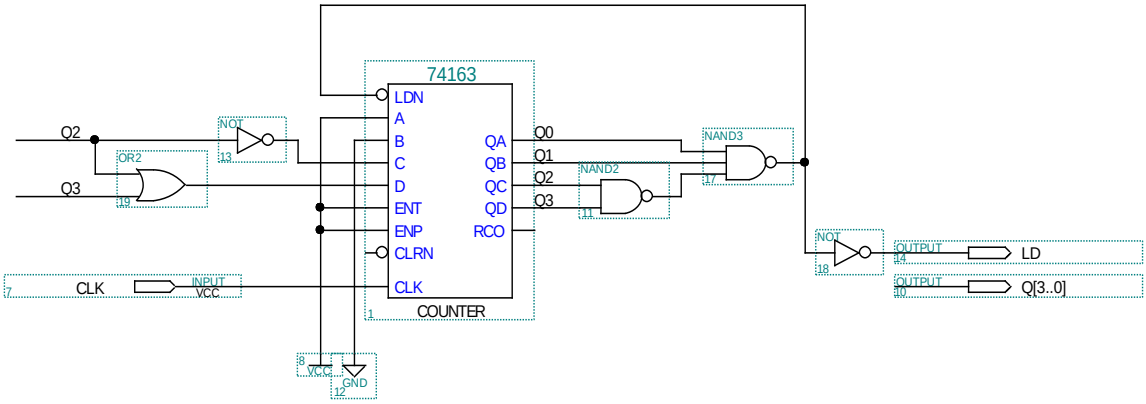
67. Determine the state diagram of the following counter. Q_1 is the MSB.



68. Excitation Table:
    a. Write down the excitation table for J-K flip-flop.
    b. Explain how this table is constructed.
    c. Explain how this table can be used to simplify your logic design.
69. Construct a D flip-flop from a J-K flip-flop. You may use additional AND, OR, NOT gates.
70. Design a counter to produce the following sequence. Use J-K flip-flops.
    00, 10, 01, 11, 00, …
71. What will this counter do?

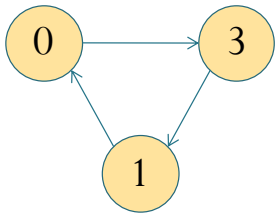


72. What will this counter do? (Difficult)



73. Counter Design:

a. Construct a counter whose counting sequence satisfies the state transition diagram below. Use D FFs.



b. Find the "complete" state transition diagram (which includes all states) for the counter you constructed in part (a).

c. Draw the waveforms of the outputs from the counter you constructed in part (a). Assume "0" is the initial state. Provide at least 6 clock periods.

d. Repeat part (a) but use J-K FFs.

e. Construct the counter as in part (a). There should be a count enable (CTEN) input as well.

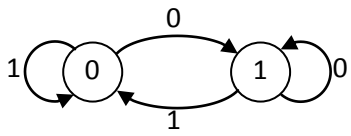
f. Construct the counter as in part (d). There should be a count enable (CTEN) input as well.

74. Design a state machine which simultaneously satisfies all of the following requirements:

a) Have one-bit input signal called W.

b) Have one-bit output signal called Y.

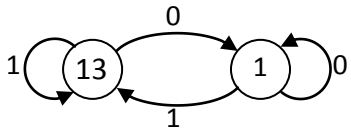
c) The counting sequence agrees with the following state diagram:



The numbers on the arrows indicate the values of W.

d) Use exactly one D flip-flop.
e) Additional AND, OR, NOT gates are allowed.

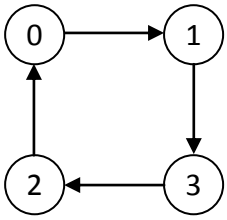
75. Design a state machine which simultaneously satisfies all of the following requirements:
    a) Have one-bit input signal called W.
    b) Have four-bit output signals called Y_3 Y_2 Y_1 and Y_0.
       Y_3 is the MSB.
    c) The counting sequence agrees with the following state diagram:



The numbers on the arrows indicate the values of W.

    d) The output is simply the unsigned binary representation of the state in the state transition diagram.
    e) Use exactly one D flip-flop.
    f) Additional AND, OR, NOT gates are allowed.

76. Design a counter which simultaneously satisfies all of the following requirements:
    a) Have no input signal.
    b) Have two-bit output signals called Y_1 and Y_0.
       Y_1 is the MSB.
    c) The counting sequence agrees with the following state diagram:



    d) Use exactly one D flip-flop and one J-K flip-flop.
    e) The counter output Y_0 is the output of the J-K flip-flop.
    f) The counter output Y_1 is the output of the D flip-flop.
    g) No additional gate allowed.

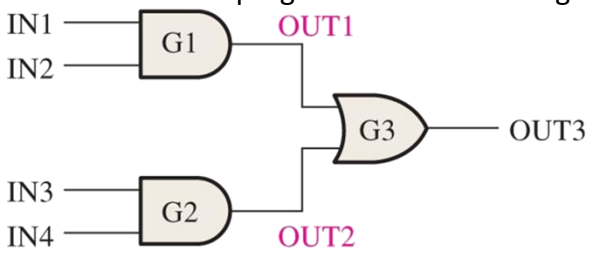
77. Compare and contrast SRAM and DRAM.
78. What is address multiplexing in DRAM? Why is it useful?
79. Compare and contrast RAM and ROM.

80. Compare and contrast word-length memory expansion and word-capacity memory expansion.
81. Show how to construct one 65536 x 8 ROM from two 65536 x 4 ROMs.
82. The starting point for the CD's data spiral is towards the center of the disc, extending outward. What are the advantages of this format?
83. To convert analog signals to digital ones, there are two important steps. They are 1) _____ and 2) _____ .
84. Analog signals (sound, image, etc) usually contain a spectrum of component frequencies. Periodic signal can be expressed in terms of its components via _____. In general, signal can be expressed in terms of its components via _____.
85. If you've ever watched a film and seen the wheel of a rolling wagon appear to be going backwards, you've witnessed _____.
86. The Nyquist frequency is defined as _____.
87. Sampling:
    a. What is the frequency of the signal $\sin(200\pi t)$?
    b. To avoid aliasing, the sampling theorem says that the sampling rate should be _____
    c. Which one(s) of the following sampling rate will experience problem with aliasing for the signal in part (a)?
        i. 10 Hz
        ii. 20 Hz
        iii. 100 Hz
        iv. 1000 Hz
        v. 10000 Hz
88. Given the following VHDL program, create the truth table that describes the logic circuit.

```
entity CombLogic is
  port (A, B, C, D: in bit; X: out bit);
end entity CombLogic;

architecture Example of CombLogic is
  begin
    X <= not((not A and not B) or (not A and not C) or (not A and not D) or
          (not B and not C) or (not B and not D) or (not D and not C));
end architecture Example;
```

89. Check the VHDL code below. It is a VHDL program for the following circuit.



Fix the missing parts.

```
architecture LogicOperation of AND_OR_Logic is
    component AND_gate is
                                                    <-- Component declaration for the AND gate
    end component AND_gate;

    component OR_gate is
      port (A, B: in bit; X: out bit);              <-- Component declaration for the OR gate
    end component OR_gate;

    signal OUT1, OUT2: bit;                         <-- Signal declaration
begin
    G1: AND_gate port map (                                  );
    G2:                                                      <-- Component instantiations
    G3: OR_gate port map (A => OUT1, B => OUT2, X => OUT3);
end architecture LogicOperation;
```